A

ARA05050S12

CATV Reverse Amplifier w/ Step Attenuator
Advanced product information
Rev. 6

FEATURES

- Integrated monolithic GaAs amplifier and step attenuator.
- Compatible with all digital and analog modulation types.
- Frequency range: 5 - 100 MHz.
- Gain: 0 - 30 dB, variable in 2 dB steps.
- 5 Volt operation.
- Low noise figure.
- Low distortion.
- Amplifier shutdown capability.
- Low cost.
- High reliability.
- Low signal to noise ratio at all gain levels.

S12C
28 Pin SSOP w/ Heat Slug

DESCRIPTION

The ARA05050 is a GaAs IC designed to perform the reverse path amplification and output level control functions in a CATV Set-Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator that is preceded by an ultra low noise amplifier stage, and followed by an ultra-linear output driver amplifier. It is capable of meeting the MCNS/DOCSIS harmonic distortion specifications while only requiring a single polarity +5V supply. This part is a single ended design that does not require an output balun to achieve -55 dBc 2nd harmonic performance at +58 dBmV output levels. Both the input and output are matched to 75 ohms. The precision attenuator provides up to 30 dB of attenuation in 2 dB increments. The ARA05050 is supplied in a 28-pin SSOP package featuring a thermal heat slug on the bottom of the package. Soldering this heat slug to the ground plane of the PC board ensures the lowest possible thermal resistance for the device resulting in a long MTF.

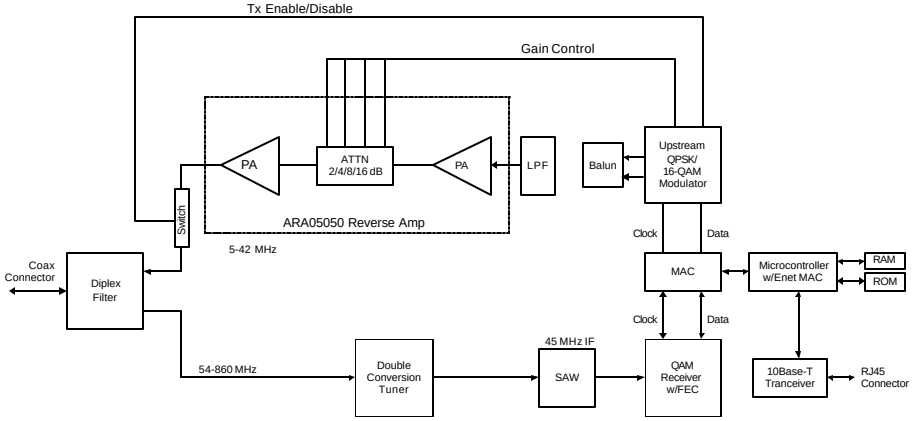


Figure 1. Cable Modem or Interactive Set-Top Box Block Diagram

**See ANADIGICS ACU50751 and ACD0900*

ELECTRICAL CHARACTERISTICS (TYPICAL) (VDD=5 VDC, TC=25 °C)

Parameter	Min	Typ	Max	Unit	Comments
Gain [1]	30	32	33	dB	At 0dB attenuation setting
Gain Flatness [1]	-	0.75	1.5	dB	5 to 100 MHz
Attenuation Steps [1] 2 dB 4 dB 8 dB 16 dB	 1.6 3.8 8.0 16.0	 1.85 4.0 8.3 16.6	 2.2 4.2 8.5 17.0	dB	5 to 42 MHz [3]
2nd Harmonic Distortion Level [2] 5 MHz 25 MHz	 - -	 -60 -63	 -55 -55	dBc	
3rd Harmonic Distortion Level [2] 5 MHz 25 MHz	 - -	 -63 -63	 -60 -60	dBc	
3rd Order Output Intercept Point	78	-	-	dBmV	
1dB Gain Compression Point	-	70	-	dBmV	
Noise Figure	-	1.7	2.5	dB	
Output Noise Power Active/No Signal/Min Attn. Setting Active/No Signal/Max Attn. Setting	 - -	 - -	 -24.6 -41.6	dBmV	Any 3200 KHz bandwidth from 5 to 42 MHz
On/Off Isolation Shut Off Stage 2 Shut Off Stages 1 & 2	 -	 30 53.5	 - -	dB	Difference in output signal level between active and standby
Input Impedance[1]	-	75	-	ohm	
Input Return Loss[1]	-	-20	-15	dB	
Output Impedance[1]	-	75	-	ohm	
Ouput Return Loss[1]	-	-20	-15	dB	
V_{DD1}, V_{DD2}	-	5	7	V	
V_{DD} Digital	-	5	-	V	
V Shutdown	-2	-	-1.5	V	
I_{DD1}	-	75	95	mA	
I_{DD2}	-	100	130	mA	
I_{DD} Digital	-	8	-	mA	
Power Consumption	-	1	1.2	W	
Attenuator Control Impedance	-	5 K	-	ohm	
Attenuator Control Logic [4] VIL VIH	 0 2.8	 - -	 0.5 6.5	Volts	

Notes:
1. As measured in ANADIGICS test fixture
2. At +58 dBmV output level into 75 ohm load
3. For higher frequencies see figures 3 & 4.
4. With 470 ohm chip resistor from pin 2 to gnd (see test circuit).

ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute Maximum	Unit
V_{DD} (Pins 4,12, 18)	9	VDC
V_{RFIN} (Pins 10, 24)	0 to -3	VDC
ATT_{IN} (Pin 3) ATT_{OUT} (Pin 26)	5	VDC
V_{ISET} (Pins 11, 25)	2	VDC
RF Input Voltage (Pins 10, 24)*	+60	dBmV
Storage Temperature	-55 to +200	°C
Soldering Temperature	260	°C
Soldering Time	5	Sec
Operating Case Temperature	-40 to +85	°C

* Blocking capacitors required

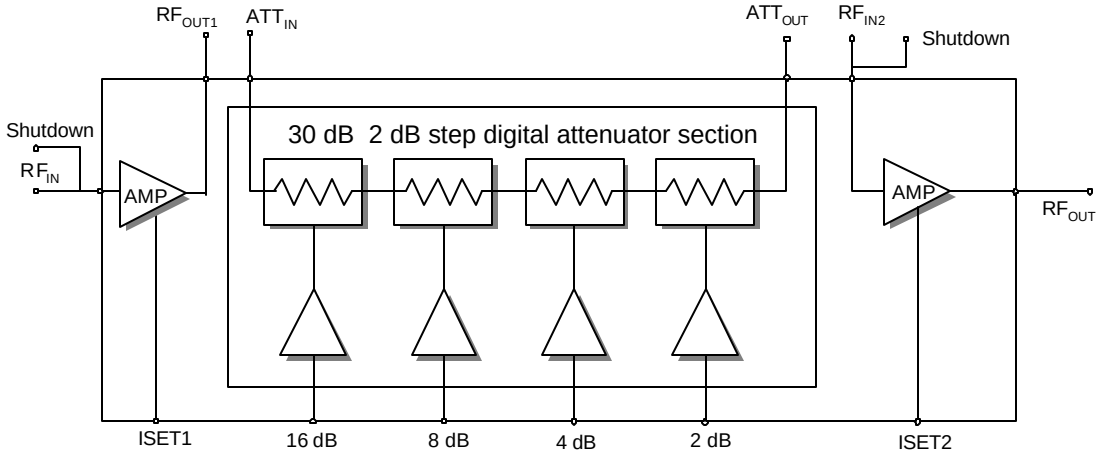


Figure 2

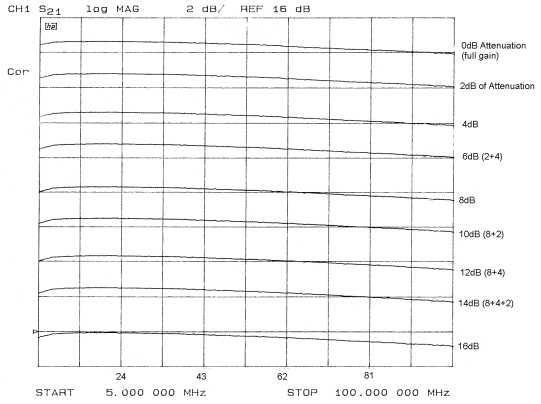


Figure 3

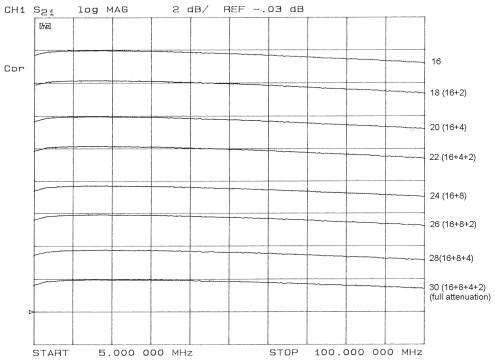


Figure 4

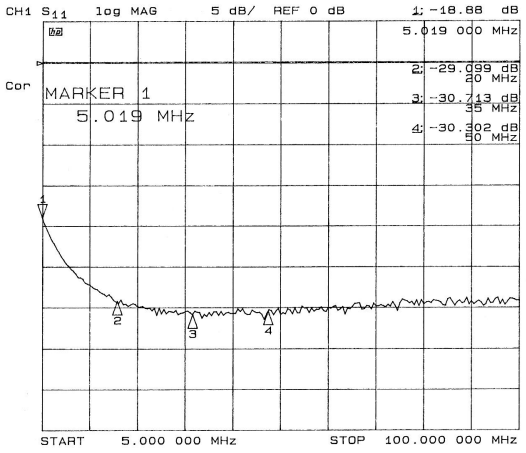


Figure 5

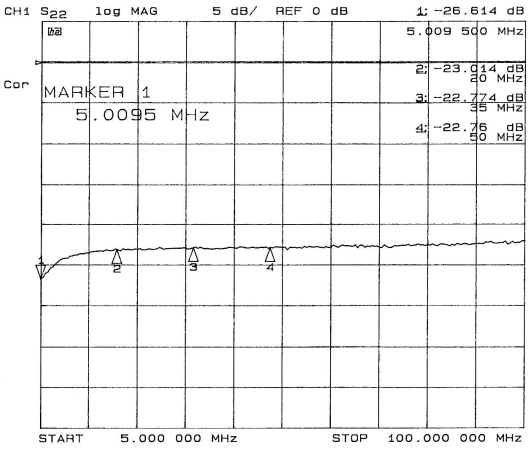


Figure 6

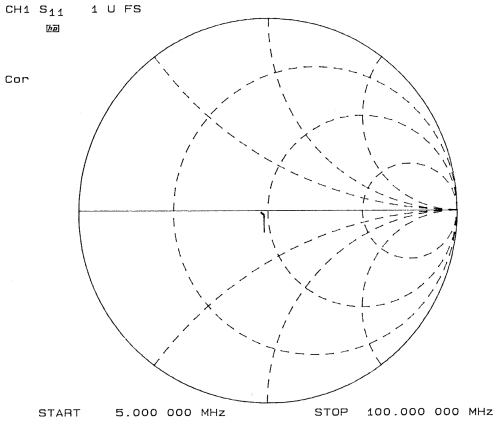


Figure 7

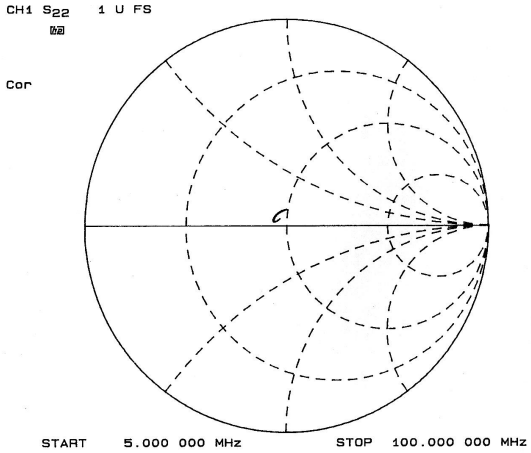


Figure 8

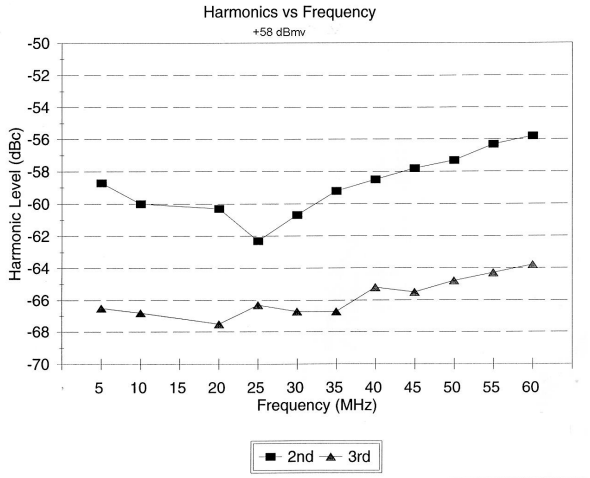


Figure 9

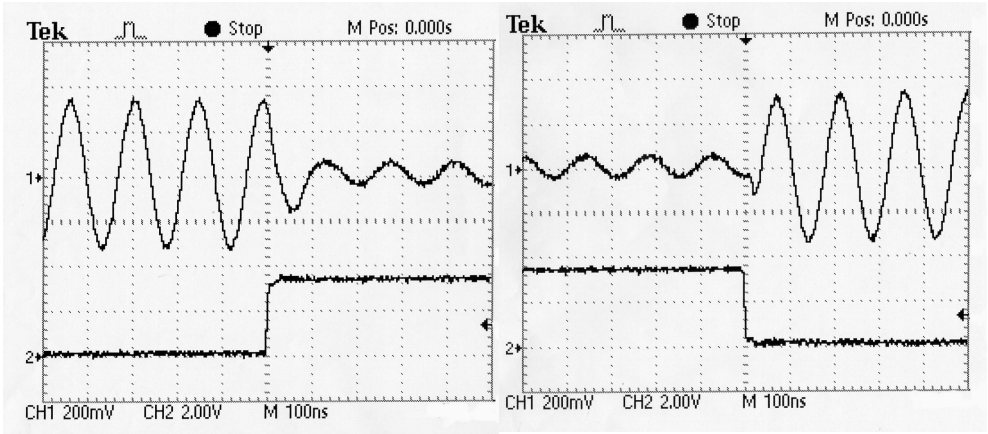


Figure 10. Attenuator Switching Speed 16 dB Step

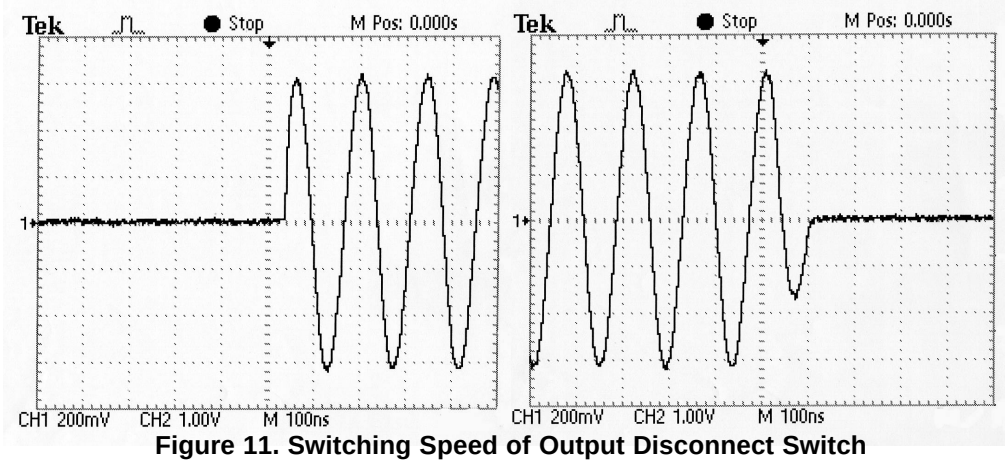
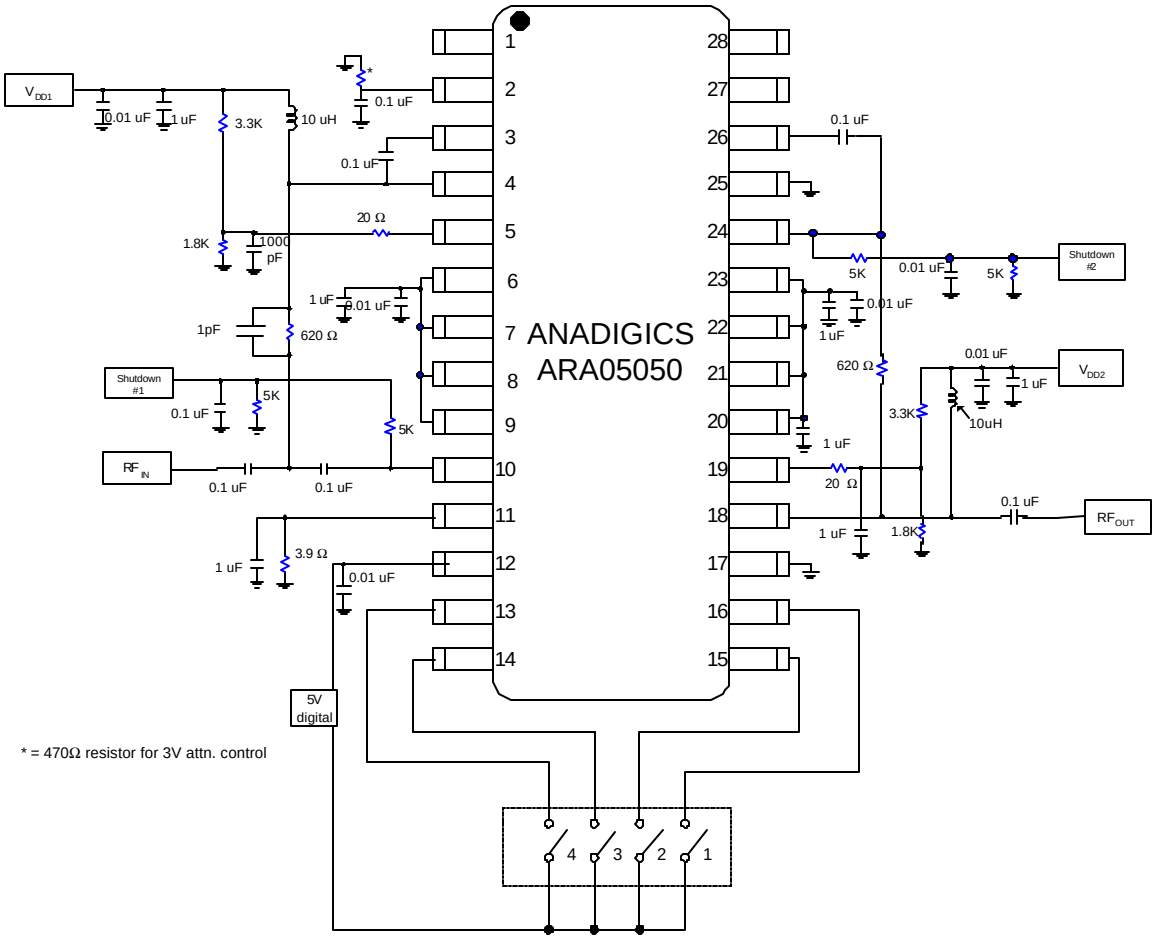


Figure 11. Switching Speed of Output Disconnect Switch

TEST CIRCUIT



DIP SWITCH LOGIC TABLE

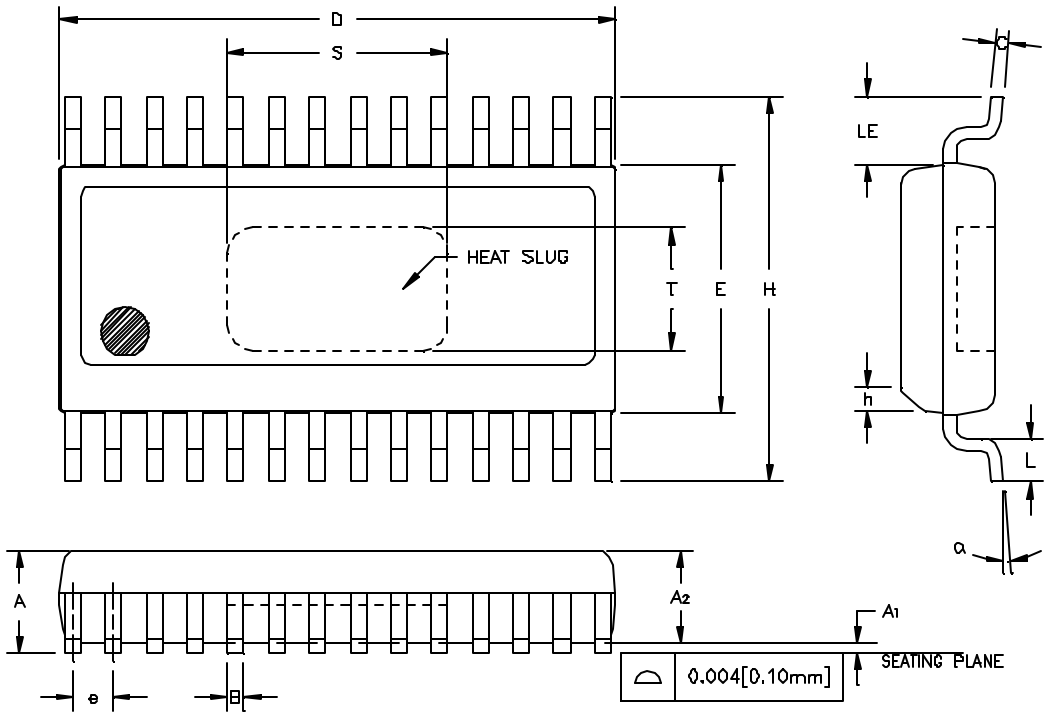
Attn (dB)	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
SW 1	X	O	X	O	X	O	X	O	X	O	X	O	X	O	X
SW 2	O	X	X	O	O	X	X	O	O	X	X	O	O	X	X
SW 3	O	O	O	X	X	X	X	O	O	O	O	X	X	X	X
SW4	O	O	O	O	O	O	O	X	X	X	X	X	X	X	X

O = Open
X = Closed

PIN DESCRIPTION

PIN	FUNCTION	DESCRIPTION
1	NC	No Connection
2	Bypass	Internal bypass. This pin must be externally ac decoupled (0.1uf cap)
3	ATT_{IN}	Attenuator Input
4	$RF_{OUT1}+V_{DD1}$	RF Output and +5v Supply for 1st Amplifier Stage
5	V_{REF1}	Reference voltage for 1st Amplifier
6,7,8,9	AC_GND	AC Ground. These pins must be externally ac decoupled (1uF and 0.01uF cap)
10	RF_{IN}	RF Input to 1st Amplifier Stage
11	I_{SET1}	Resistor set current for 1st Amplifier
12	5V digital	5 volts digital supply voltage
13	16 dB	16 dB Attenuator Control Parallel data input
14	8 dB	8 dB Attenuator Control Parallel data input
15	4 dB	4 dB Attenuator Control Parallel data input
16	2 dB	2 dB Attenuator Control Parallel data input
17	Dig GND	Digital Ground
18	$RF_{OUT}+V_{DD2}$	RF Output and $+V_{DD2}$ V Supply for 2nd Amplifier Stage
19	V_{REF2}	Reference voltage for 2nd Amplifier
20,21,22,23	AC_GND	AC Ground. These pins must be externally ac decoupled (1uF and 0.01uF cap)
24	RF_{IN2}	RF Input to 2nd Amplifier Stage and Shutdown pin for 2nd Amplifier
25	I_{SET2}	Resistor set current for 2nd Amplifier (ground for max performance)
26	ATT_{OUT}	Attenuator Output
27	NC	No Connection
28	NC	No Connection

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX	MIN	MAX	
A	0.058	0.068	1.47	1.73	
A1	0.000	0.004	0.00	0.10	
A2	0.054	0.060	1.37	1.52	
B	0.008	0.014	0.20	0.35	5
C	0.007	0.012	0.18	0.30	5
D	0.385	0.393	9.78	9.98	2
E	0.151	0.157	3.84	3.99	3
e	0.025 BSC		0.64 BSC		4
H	0.228	0.244	5.79	6.20	
h	0.015x45°		0.38x45°		
L	0.016	0.032	0.41	0.81	
LE	0.042	—	1.07	—	
α	0°	8°	0°	8°	
S	0.105	0.135	2.67	3.43	6
T	0.045	0.075	1.41	1.91	6

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.0035 [0.089mm].
5. LEAD WIDTH "B" AND THICKNESS "C" MAX. DIMENSION IS AFTER PLATING
6. DIMENSIONS "S" AND "T" INDICATE EXPOSED SLUG AREA

0-012

LAYOUT CONSIDERATIONS
There are two issues that must be taken into consideration when doing the PCB layout. The first is thermal management, and the second is RF related.

THERMAL LAYOUT CONSIDERATIONS
The ARA05050 will typically dissipate 0.9W, and as high as 1.2W. Since the interior of most set-top boxes, and cable modems as well typically are at +70°C, consideration must be given to providing an adequate heat sink for the die to obtain the maximum MTF possible. To this end the ARA05050 incorporates a heat slug in the bottom of the package. This provides a low thermal resistance path from the die to the outside of the package. The typical thermal rise from the heat slug to the junction is 35°C/W. However, this is only half of the equation. Adequate heat sinking must be applied to the heat slug for thermal dissipation. Providing a metalized pad with via holes under the package will do this (see Figure 14). The via holes should connect to the ground plane of the PCB. The part is then soldered to this pad during assembly.

EXTERNAL CIRCUITRY
Output Disconnect Switch:
For MCNS/DOCSIS applications an external switch to disconnect the output of the ARA05050 from the diplexer is required. This switch is needed because of the output noise requirement between bursts, and because of the requirement that any shutdown transient not exceed 7mV. The switch shown in Figure 12 meets these conditions because it does not switch any current, or voltage, on the output line. The series FET provides 35 dB of isolation, while the shunt FET insures that the diplexer remains terminated into a 75 ohm impedance. Since the switch does not draw any current, it may be driven directly from a low power CMOS logic inverter; however the control voltages must be +5V. When the switch is in the open state, it is good general practice to set the programmable attenuator to its maximum attenuation setting. This will increase the isolation between the cm output and upstream modulator, and provide the first stage amplifier with a 75 ohm termination.

Shutdown of the ARA05050:
In some applications it may be desirable to shut the ARA05050 down for power saving. This can be done by applying a negative voltage to pin 10 to shut down the input stage, and to pin 24 to shut down output stage (see Figure 13). Shutting down both amplifier stages will reduce the current drawn from the +5V supply to typically 10 mA. If only one stage is shutdown, it is recommended that the programmable attenuator be set to a minimum of 16 dB to provide a good impedance match to the remaining stage.

RF LAYOUT CONSIDERATIONS
The ARA05050 is a power amplifier designed for driving a 75ohm load. Since this part connects the transmitter to the cable system, typically via a diplexer, it is an analog device operating at RF frequencies. This means that the layout of the PCB will have an effect on the system performance. The first consideration in RF layout are the connections to ground. These must be low impedance, and as short as possible. The best way to do this is to use as large a via hole as possible, located as close as possible to connect to the ground plane. Specifically, care should be given to the layout of the following connections (the traces leading from the following pins to their respective components should be as low as impedance as is practical.):

Pins 5 & 19: the 20 ohm chip resistor should be as close as possible to the pins and the 1 uF capacitor should be kept close to the 20 ohm resistor.

Pins 6–9 & 20–23: the capacitors should be kept close to the pins.

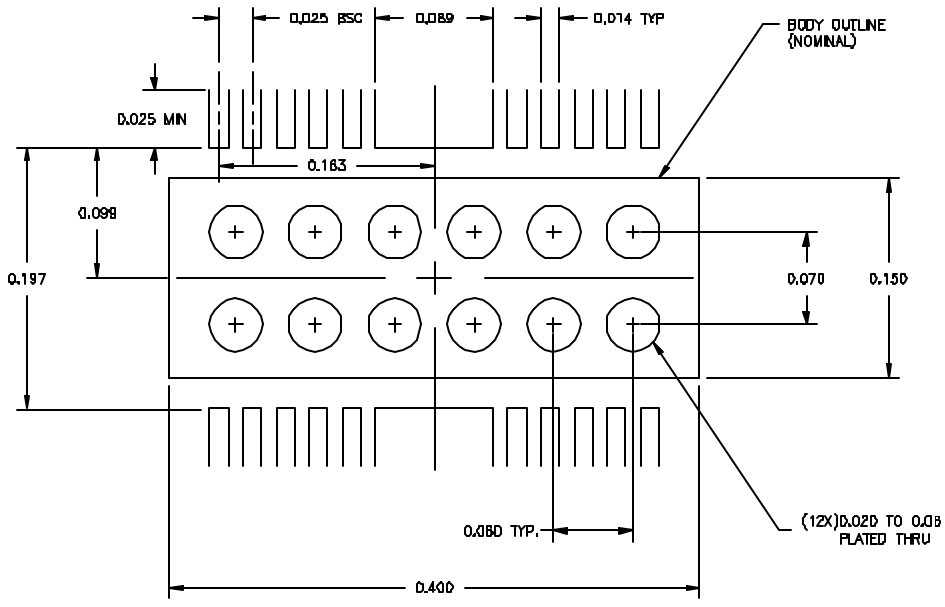
Pin 11: the 1uF bypass capacitor should be kept close to the pin.

Pin 12: the bypass capacitor at this node should be reasonably close ot the pin.

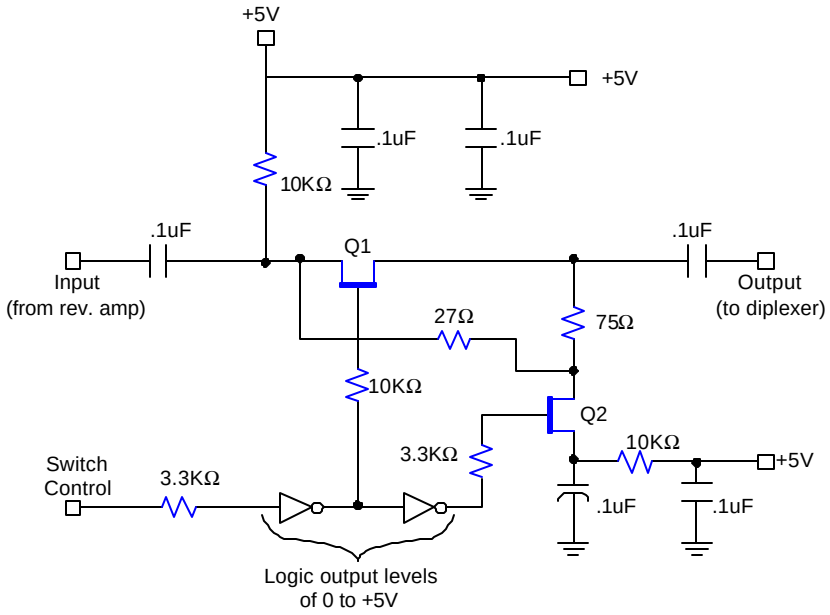
The path leading between **pins 4–10**, and the path between **pins 18–24**, should be kept as short as possible.

The bypass capacitors on the Vdd lines should be located as close as possible to the 10 uH inductors.

The traces leading to the RF input, and leading away from the RF output, should be 75 ohms. Care should be taken to keep other traces, which may have clock signals on them, as far away as is practical to prevent unwanted coupling onto the signal line.



HOLE PATTERN UNDER ARA05050



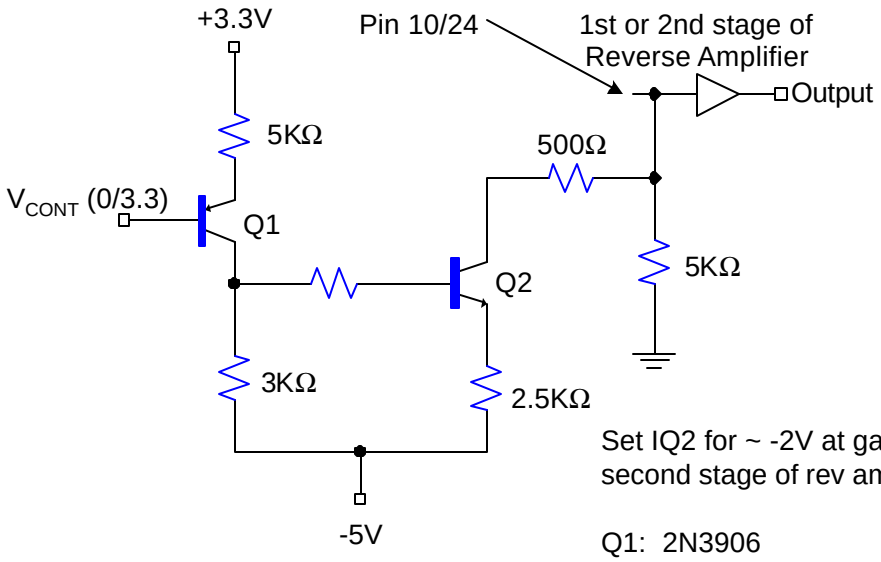
Q1/Q2 are
AF002C4 (Alpha)

Insertion Loss
@ 45 MHz: 0.1dB

Isolation
@ 45 MHz: 38dB

2nd Harmonic
@ +58 dBmV > 70dBc

Figure 12. Output Disconnect Switch



Set IQ2 for ~ -2V at gate of
second stage of rev amp

Q1: 2N3906
Q2: 2N3904

Figure 13

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